IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Bruce *et al.*	Examiner:	Charioui, M.
Serial No.:	09/586,518	Group Art Unit:	2857
Filed:	June 2, 2000	Docket:	AMDA.455PA (TT3843)
Notice of Allow. Date:	June 25, 2004	Confirmation No.:	5747
Due Date:	September 27, 2004		
Title:	RESISTIVITY ANALYSIS		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this communication is being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 21, 2004.

By: Rennae Johnson
Rennae Johnson

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We are transmitting herewith the attached:

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- ☒ Please charge Deposit Account No. 01-0365 (TT3843) the amount of $1,330.00 for the Issue Fee.
- ☒ Part B-Issue Fee Transmittal
- ☒ 11 Sheets of Formal Drawings
- ☒ "Fee Address" Indication Form
- ☒ Amendment After Allowance
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Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers.

CRAWFORD MAUNU PLLC
1270 Northland Drive
Suite 390
St. Paul, MN 55120
(651) 686-6633

By: _____
Name: Robert J. Crawford
Reg. No.: 32,122

CRAWFORD PLLC
CLIENT REF. NO. TT3843
DATE SENT 09/21/04
INITIALS RJ

Exhibit D

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together w:___pplicable fee(s), to: Mail **Mail Stop ISS\ ___EE**
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7590 06/25/2004

Crawford PLLC
1270 Northland Drive
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Rennae Johnson (Depositor's na
Rennae Johnson (Signat
09/21/04 (D

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/586,518	06/02/2000	Michael R. Bruce	AMDA.455PA	5747

TITLE OF INVENTION: RESISTIVITY ANALYSIS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1330	$0	$1330	09/27/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHARIOUI, MOHAMED	2857	702-117000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Advance Micro Devices, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Sunnyvale, CA

Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☒ corporation or other private group entity ☐ governm

4a. The following fee(s) are enclosed:

☒ Issue Fee

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Director for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) _____ (Date) 9/21/2004

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PTO/SB/47 (05-03)
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in the following listed application(s) for which the Issue Fee has been paid or patent(s).

PATENT NUMBER (if known)	APPLICATION NUMBER
	09/586,518 filed 06/02/2000 Applicant: Bruce et al.

Completed by (check one):

[ ] Application/Inventor

[X] Attorney or Agent of record 32,122 (Reg. No.)

[ ] Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

Assignee recorded at Reel _____ Frame _____

Signature

Robert J. Crawford
Typed or printed name

(651) 686-6633
Requester's telephone number

09/21/04
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

[X] * Total of 1 forms are submitted.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 21, 2004.

By: Rennae Johnson
Rennae Johnson

AMENDMENT AFTER ALLOWANCE UNDER 37 C.F.R. § 1.312

MAIL STOP ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notice of Allowance, dated June 25, 2004, please amend the application as follows:

CRAWFORD PLLC
CLIENT REF. NO. TT3843
DATE SENT 09/21/04
INITIALS RJ

In the Specification

At page 1, lines 8 – 15, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

The following patent documents are related to the present invention and are hereby incorporated by reference in their entirety; these U.S. Patent Applications are identified by their Serial Nos. as follows: 09/034,546, filed on March 3, 1998 and entitled "Thermally-induced Voltage Alteration (TIVA)", now U.S. Patent No. 6,078,183; and 09/586,505, entitled "Method and Apparatus for Analyzing Functional Failures In Integrated Circuits", now U.S. Patent No. 6,549,022~~(Docket No. SD6542S93805)~~ and 09/586,572, entitled "Data Processing Device Test Apparatus and Method Therefor", now U.S. Patent No. 6,546,513,~~(Docket No.184-P017US),~~ which have been concurrently filed herewith.

At page 2, lines 6 – 14, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

Many integrated circuit dies include circuits that are suspect defects, and these defects can recover or fail under particular operating conditions and at higher temperatures. For instance, circuit sites exhibiting temperature sensitive defects, such [[a]]as resistive connection, can recover when heated. Traditionally, isolation of IC defects has been attempted by operating the die in a manner that causes a failure to occur and by attempting to attribute the failure to a malfunctioning device in the IC. Such electrical testing, however, does not always work because many failures and malfunctions can result from a variety of different types of defects and defects at non-suspect circuitry locations.

At page 7, lines 20 – 23 and page 8, lines 1 – 5, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

One example of such operational failure results is when an electrical signal arrives at a destination too early or too late, resulting in an incorrect value of an output state of the IC. Circuit elements that can be involved with such failures include, for example, switching transistors or functional circuit blocks that switch between logic states at a rate that is slower than normal, and interconnections in the IC which have a resistance larger than an expected value. In general, anything within an IC that results in or contributes to a particular signal within the IC being advanced or delayed in propagation by one or more clock cycles, compared with the time at which the signal should appear, can result in an operational failure in the IC.

At page 10, lines 17 – 23 and page 11, lines 1 – 9, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

Operating an IC die under a failure condition can be accomplished in various manners. In some instances, the die is allowed to operate under normal operating conditions and is analyzed therefrom. In other instances, the die is operated under conditions that are selected to cause a failure condition. For example, the die can be operated under conditions that include selected clock speeds, temperatures, logic states, or other parameters that have been associated with a defect. In addition, the die can be operated using a selected test pattern that includes a pause in the signal to provide the die time to cool between cycles when being operated in a loop. Once a particular failure is identified to occur under a particular operating condition, that operating condition can be used to test the die under similar conditions to cause the failure to recur. In addition, the operating conditions can be selected so that the die fails at a selected failure rate, and variations in the failure rate that result in response to the application of heat can be used to analyze the die. For more information regarding the operation of an die die under failure conditions, reference may be made to the above-referenced U.S. Patent Application No. 09/034,546, now U.S Patent No. 6,078,183 entitled "Thermally-induced Voltage Alteration (TIVA)."

At page 14, lines 10 – 17, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

Also, a hardware latch, such as the latch shown in FIG. 5, or a software latch can be used to capture the logic state associated with the failure transition. One advantage of using a software latch is that the IC being tested is not placed under a load at the pin from which a signal is obtained. This is useful because loading the I/O pin can cause changes in the timing that can require a re-characterization of the IC being tested. For information regarding manners in which to test IC timing characteristics, reference may be made to U.S. Patent Application Serial No. ~~09/___,___~~09/586,572 entitled "Data Processing Device Test Apparatus and Method Therefor", now U.S. Patent No. 6,546,513. ~~(Docket No.184-P017US).~~

Remarks

Amendment of the application is appropriate for grammatical accuracy.

A favorable response is earnestly requested. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is encouraged to contact the undersigned at 651/686-6633.

Respectfully submitted,

CRAWFORD MAUNU PLLC
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By: _____
Name: Robert J. Crawford
Reg. No.: 32,122